

EAST - [10709372.wsp:1]

File View Edit Tools Window Help

☐ Drafts
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 L3: (138) memory and ((source drain source/drain) with trench\$2) and (charge-trapping charge near ...
 L4: (6) "6486028"
 L2: (93) memory and ((source drain source/drain) with trench) and (charge-trapping charge near tr...
 L5: (24) memory and trench and ((charge-trapping charge near trap\$4) and (source/drain source and...
☐ Failed
 memory and trench and (charge-trapping charge near trap\$4 and (source/drain source drain)
☐ Saved
 S1: (439) memory and trench and (charge-trapping charge near trap\$4 and (source/drain source drain))
 S2: (433) memory and trench and ((charge-trapping charge near trap\$4) and (source/drain source an...
 S4: (24) memory and trench and ((charge-trapping charge near trap\$4) and (source/drain source dra...
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☐ Plurals
 Date Highlight all OR daily
 memory and ((source drain source/drain) with trench\$2) and (charge-trapping charge near trap\$4)

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050012141 A1	20050120	30	Asymmetric band-gap engineered nonvolatile memory device	257/318	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20050006710 A1	20050113	14	Semiconductor memory with virtual ground architecture	257/390	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20050003613 A1	20050106	8	Method for fabricating a semiconductor memory having charge trapping memory	438/257	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20050001258 A1	20050106	21	Apparatus and method for split gate NROM memory	257/314	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040232472 A1	20041125	57	Nonvolatile semiconductor memory and method of manufacturing the same	257/314	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040232471 A1	20041125	60	Semiconductor integrated circuit device and its manufacturing method	257/314	257/324; 257/332;
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040232470 A1	20041125	12	Memory device having a P+ gate and thin bottom oxide and method of erasing same	257/311	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040229437 A1	20041118	10	Non-volatile memory device having a nitride barrier to reduce the fast erase	438/265	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20040214379 A1	20041028	127	Rail stack array of charge storage devices and method of making same	438/149	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20040212006 A1	20041028	18	Non-volatile memory cells utilizing substrate trenches	257/315	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20040206996 A1	20041021	126	Dense arrays and charge storage devices	257/296	